Amendments to the Specification:

Please replace paragraph [0015] with the following amended paragraph:

[0015] Figure 1 depicts a magnetic memory 10 that may be integrated as an array ~~12~~ on an integrated circuit. In general, the array includes memory elements 14A-I, which may be magnetically coupled to write lines as shown by the dashed lines. The magnetic memory elements may be modeled using various devices such as capacitors, resistors, inductors, tunnel junctions in series with diodes, or other combinations of integrated circuit elements. The write lines may be organized in columns 16A-D and rows 18A-D. Accompanying circuitry 19 may be coupled to write lines 16 and 18, and may assist in writing data to the array 12. Although not shown in Figure 1, read lines may be electrically coupled to the memory elements 14A-I in order to perform read operations.

Please replace paragraph [0017] with the following amended paragraph:

[0017] Figure 2 shows an embodiment of the present invention that may be used as a magnetic memory write line driver. Circuit 30 may provide desired current control in a magnetic memory write line 32 while minimizing the amount of overhead voltage utilized and simplifying overall circuit design. Memory write line 32 may be magnetically coupled to magnetic memory element 34. The supply voltage, indicated as V_{DD}, may be electrically coupled to the source terminals of a plurality of p-channel MOSFETs 36. MOSFETs~~Transistors~~ 36 may have their drains electrically coupled to a write line 32, which may be represented as resistive element R_W. Write line 32 may also be electrically coupled to the drain terminal a plurality of n-channel MOSFETs 38, and the source connection of MOSFETs~~transistors~~ 38 may be electrically coupled to ground.

Please replace paragraph [0019] with the following amended paragraph:

[0019] As switches SP_X couple the gates of transistors 36 to ground, the gate-to-source voltage of transistors 36 may be equal to $-V_{DD}$, which is the maximum voltage available in circuit 30. Likewise switches SN_X may couple the gates of transistors 38 to V_{DD}, which also may yield the maximum possible gate-to-source

voltage available in circuit 30. In general, when the gate-to-source voltage of a transistor is at a maximum, the resistance may be at a minimum value. Since transistors 36 and 38 may be configured with a minimal resistance value, they may have a lower drain-to-source voltage than other solutions. ~~For example, the drain-to-source voltage of transistors 36 and 38 may be lower than that of transistor 26 in circuit 20.~~ Accordingly, circuit 30 may be able to control the amount of current in write line 32 by using less overhead voltage than would otherwise be required.~~is used by circuit 20.~~ Although V_{DD} may supply a variable current to the write line, the voltage supplied by V_{DD} does not need to be varied in order to supply the variable current to the write line.

Please replace paragraph [0025] with the following amended paragraph:

[0025] The memory disclosed herein, and the methods for controlling current in memory write lines may be used in a computer system. Figure 4 illustrates an exemplary computer system 100. The computer system of Figure 4 includes a Central Processing Unit "CPU" 102 that may be electrically coupled to a bridge logic device 106 via a CPU bus. The bridge logic device 106 is sometimes referred to as a "North bridge." The North bridge 106 electrically couples to a main memory array 104 by a memory bus, and may further electrically couple to a graphics controller 108 via an advanced graphics processor ("AGP") bus. The main memory array 104 may be a magnetic memory array utilizing the disclosed methods for controlling the write line current. The North bridge 106 couples CPU 102, memory 104, and graphics controller 108 to the other peripheral devices in the system through, for example, a primary expansion bus ("BUS A") such as a Peripheral Component Interconnect ("PCI") bus or an Extended Industry Standard Architecture ("EISA") bus. Various components that operate using the bus protocol of BUS A may reside on this bus, such as an audio device 114, a IEEE 1394 interface device 116, and a network interface card ("NIC") 118. These components may be integrated onto the motherboard, as suggested by Figure 4, or they may be plugged into expansion slots 110 that are connected to BUS A.

Please replace paragraph [0026] with the following amended paragraph:

[0026] If other secondary expansion buses are provided in the computer system, another bridge logic device 112 may be used to electrically couple the primary expansion bus ("BUS A") to the secondary expansion bus ("BUS B"). This bridge logic 112 is sometimes referred to as a "South bridge." Various components that operate using the bus protocol of BUS B may reside on this bus, such as a hard disk controller 122, a system Read Only Memory ("ROM") 124, and Super Input/Output ("I/O") controller 126. Slots 120 may also be provided for plug-in components that comply with the protocol of BUS B.